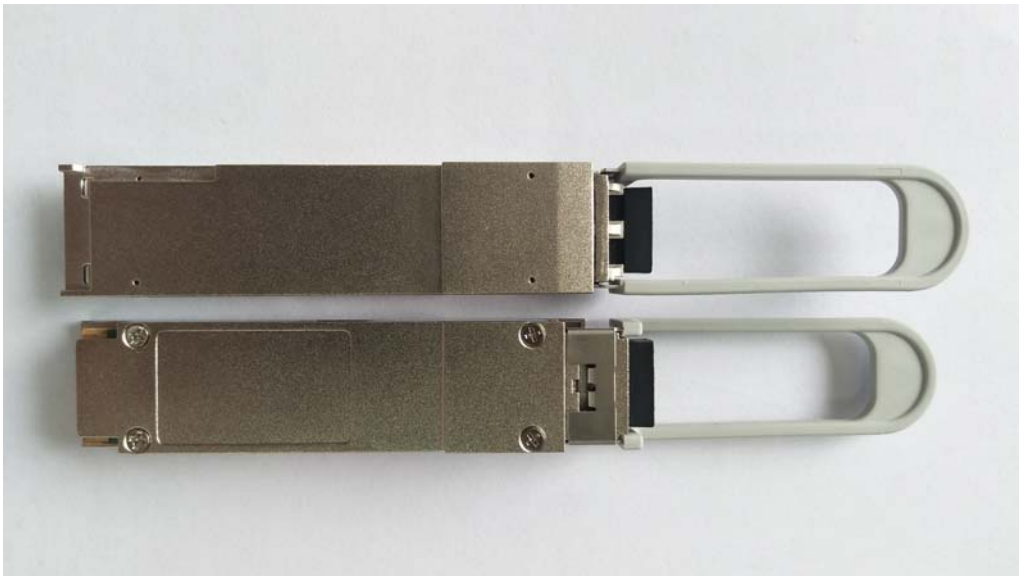
Product Specification Sheet

40G-SR-BD-S1

RoHS Compliant 40Gb/s QSFP+ BIDI 850nm/900nm 100m Optical Transceiver



Product Features

●Supports 1.06 to 10.5Gb/s bit rates per Channel
●Hot pluggable QSFP+ form factor
●VCSELtransmitters and PIN receiver
●Applicable for 100m on OM3 MMF,150mon OM4 MMF.
●Utilizes a standard LC duplex fiber cable allowing reuse of existing cable infrastructure
●Built-in digital diagnostic functions
●Low power consumption, < 3.5W
●Unretimed XLPPI electrical interface
●Compliant to QSFP+ SFF-8436 Specification
●Operating case temperature: -5°C to 80 °C

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Applications

●40GBASE-SR4 40G Ethernet
●Datacom/Telecom switch & router connections
●Data Aggregation and Backplane Applications
●Proprietary Protocol and Density Applications

Product Descriptions

40G-SR- BD-S1 is transmitter portion of the transceiver (see Fig-ure 1) incorporates a 4-channel XLPPI input buffer, elec-trical multiplexer, two laser drivers and two high speedVCSELs (Vertical Cavity Surface Emitting Laser). The trans-mitter is designed for EN 60825 and CDRH Class 1M eye safety compliance. The Tx Input Buffer provides XLPPI compatible differential inputs presenting a nominal dif-
ferential input impedance of 100 Ohms. AC coupling capacitors are located inside the QSFP+ module and arenot required on the host board. For module control and interrogation, the control interface (LVTTL compatible) in-corporates a Two Wire Serial (TWS) interface of clock and data signals.
The optical receiver portion of the transceiver (see Figure1) incorporates two high speed PIN photodiodes, TIAs, signal processors, electrical de-multiplexer and 4 chan-nel electrical output buffer blocks. The Rx Output Buffer provides XLPPI compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially termi- nated with 100 Ohms. AC coupling capacitors are located inside the QSFP+ module and are not required on the hostboard.The electrical output will squelch for loss of input signal (unless squelch is disabled) and channel de-activation through TWS interface. To reduce the need for polling, a hardware interrupt signal INTL is provided to inform hosts of an assertion of LOS or Tx_FAULT.

Functional Diagram

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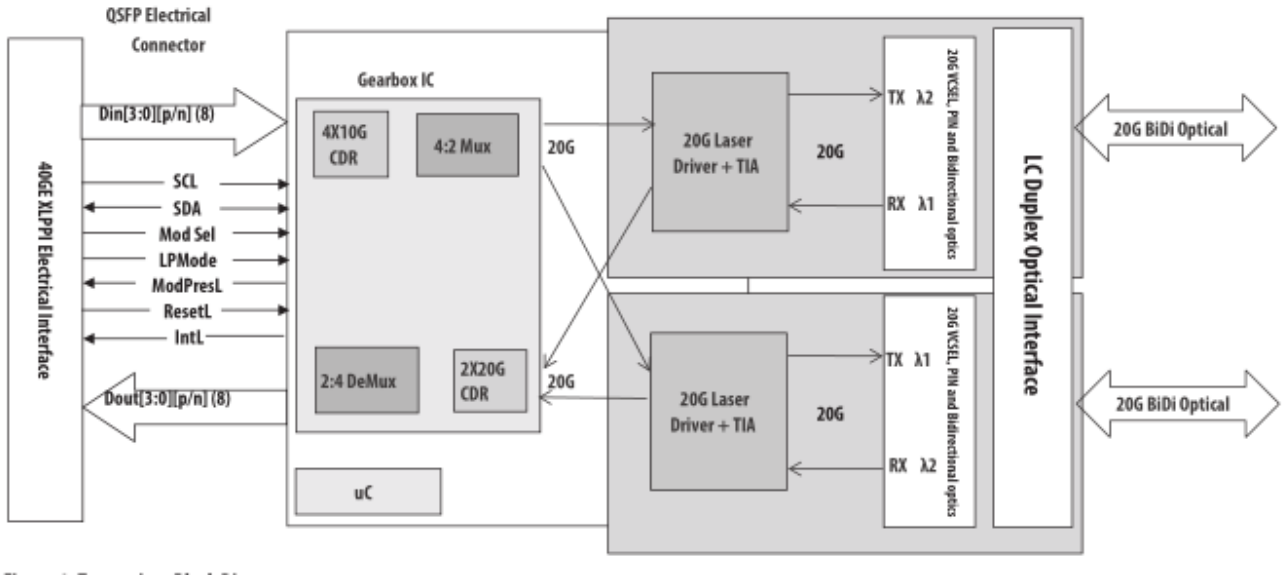

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	Vcc	-0.5	3.6	V	
Storage Temperature	Ts	-40	85	°C	
Relative Humidity	RH	0	85	%	
Damage Threshold, per Lane	DT	3.4		dBm	
Transceiver Power Consumption			3.5	W	
Transceiver Power Supply Current			1150	mA	
Transceiver Power On Initialization Time	t PWR INIT		2000	ms	1

Note:

1. Power On Initialization Time is the time from when the supply voltages reach and remain above the minimum Recommended Operating Conditions to the time when the module enables TWS access. The module at that point is fully functional.

General Operating Characteristics

Parameter	Value	Unit	Note
Module Form Factor	QSFP+		
Number of Lanes	4 Tx and 4 Rx		
Maximum Aggregate Data Rate	42.0	Gb/s	
Maximum Data Rate per Lane	10.5	Gb/s	
Protocols Supported	Typical applications include 40G Ethernet, Infiniband, Fibre Channel, SATA/SAS3		
Electrical Interface and Pin-out	38-pin edge connector ,Pin-out as defined by the QSFP+ MSA		
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		

Parameter	Symbol	Min	Typ	Max	Units	Note

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Bit Rate per Lane	B_R	1062		10500	Mb/sec	1
Bit Error Ratio	B_{ER}			10-12		2
Distance on OM3 MMF (CDS1)	D_1			100	meters	3
Distance on OM4 MMF (CDS1)	D_2			150	meters	3

Notes:
1. Compliant with 40G Ethernet. Compatible with 1/10 Gigabit Ethernet and 1/2/4/8/10G Fibre Channel.
2. Tested with a PRBS 2^{31-1} test pattern.
3. Per 40GBASE-SR4, IEEE 802.3ba,Belong to part No: OLSQ854XM-CDS1

Optical Characteristics ($T_{OP(C)}$ = 0 to 70 ℃, V_{CC} = 3.13 to 3.47 V)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Transmitter						
Operating Wavelength1	λ	840	850	860	nm	
Operating Wavelength2	λ	882	900	918	nm	
Ave. output power (Enabled)1	P_{AVE}	-4		5	dBm	
Ave. output power (Enabled)2	P_{AVE}	-4		5	dBm	
Difference in launch power between any two lanes (OMA)	D_L			4	dB	
Extinction Ratio	E_R	3	4.5		dB	
Peak power, each lane	P_P			7	dBm	
Dispersion penalty, each lane	T_{DP}			3.5	dB	
Average launch power of OFF transmitter, each lane	P_{OFF}			-30	dB	
LOS Assert Threshold: Tx Data Input Differential Peak-to-Peak Voltage Swing	Δ Vdi pp los	-40	80	190	mVpp	
Optical rise and fall time, 20-80%			21		ps	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4					Hit Ratio = 5x10-5
Receiver						
Operating Wavelength1	λc		850		nm	
Operating Wavelength2	λc		900		nm	
Stressed receiver sensitivity in OMA(OLSQ854XM-CDS1)	P_{SEN}			-7.1	dBm	1
Stressed receiver sensitivity in OMA(OLSQ904XM-CDS1)	P_{SEN}			-7.7	dBm	
Receiver Reflectance	R_{rx}			-12	dB	
LOS Assert	Pa	-30		-9.1	dBm	
LOS De-assert 850nm	Pd			-8.6	dBm	
LOS De-assert 900nm	Pd			-8.6	dBm	
LOS Hysteresis	Pd-Pa	0.5			dB	

Notes:
1.Measured with conformance test signal at TP3 for BER = $1e^{-12}$ Receiver Characteristics

Pin Defintion And Functions

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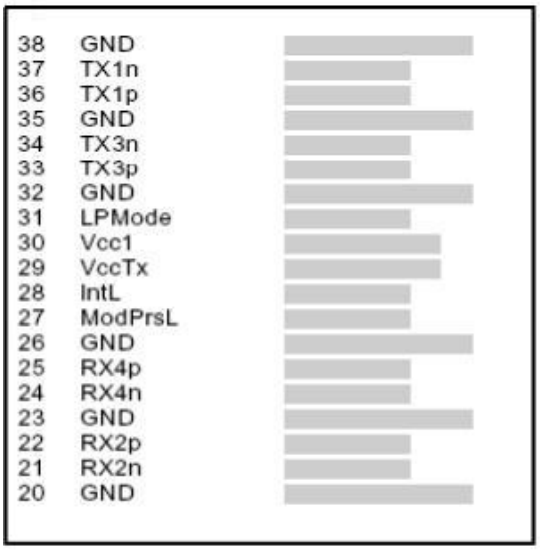
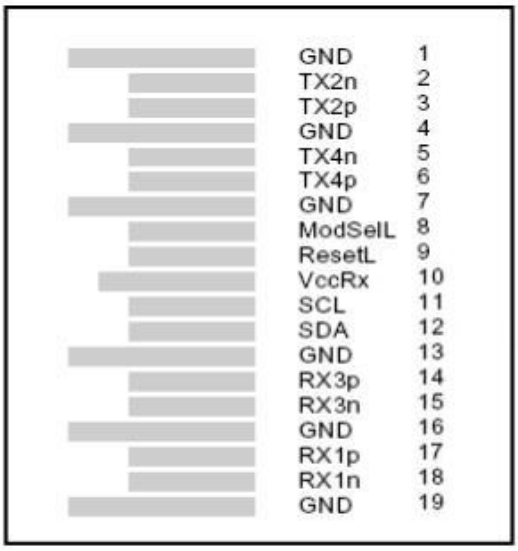


Top side



Bottom side

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	1
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver	Non-Inverted
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	

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29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. Circuit ground is internally isolated from chassis ground.

Other Pin Description:

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Rayoptek PSM IR4operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

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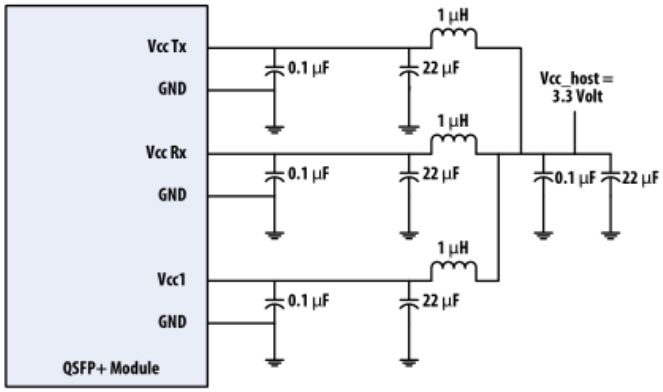
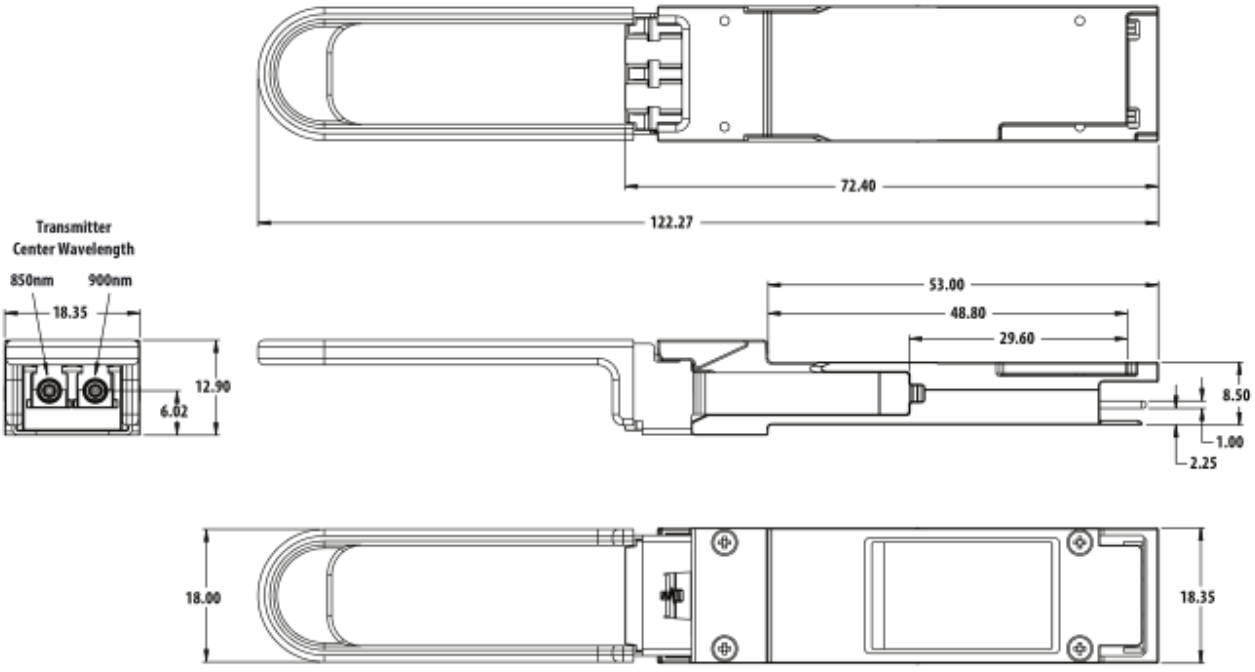


Package Dimensions



Ordering Information

Part Number	Description

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40G-SR- BD-S1	QSFP+,40Gb/s, BIDI 850nm/900nm, 100m（OM3）, 0~70℃ LC

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